Computer Organization and Architecture Lab

Assignment - 3 Part-2

Group number: 65

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Part-2 Carry Look- Ahead Adders

1. 4- Bit Carry Look-Ahead Adder

The prominent difference between a 4-Bit RCA and a 4- Bit CLA is that a CLA calculates all carries simultaneously instead of waiting for the carry from the previous block to be passed to the current block, thereby, reducing the delay in calculation of sum. Ci that is carry when ith bit of inputs are added can be represented in the form of C0 (initial carry bit).

The logic for CLA for 2 4-Bit input X and Y is shown as:

G[i] = X[i] & Y[i]

P[i] = X[i] **⊕** Y[i]

Where Gi denotes whether X[i] and Y[i] upon addition generate a carry on their own and Pi denotes whether the carry from previous block will be propagated forward or not.

Let C0  be the initial input carry bit.

Sum[i] = P[i] **⊕** C[i]

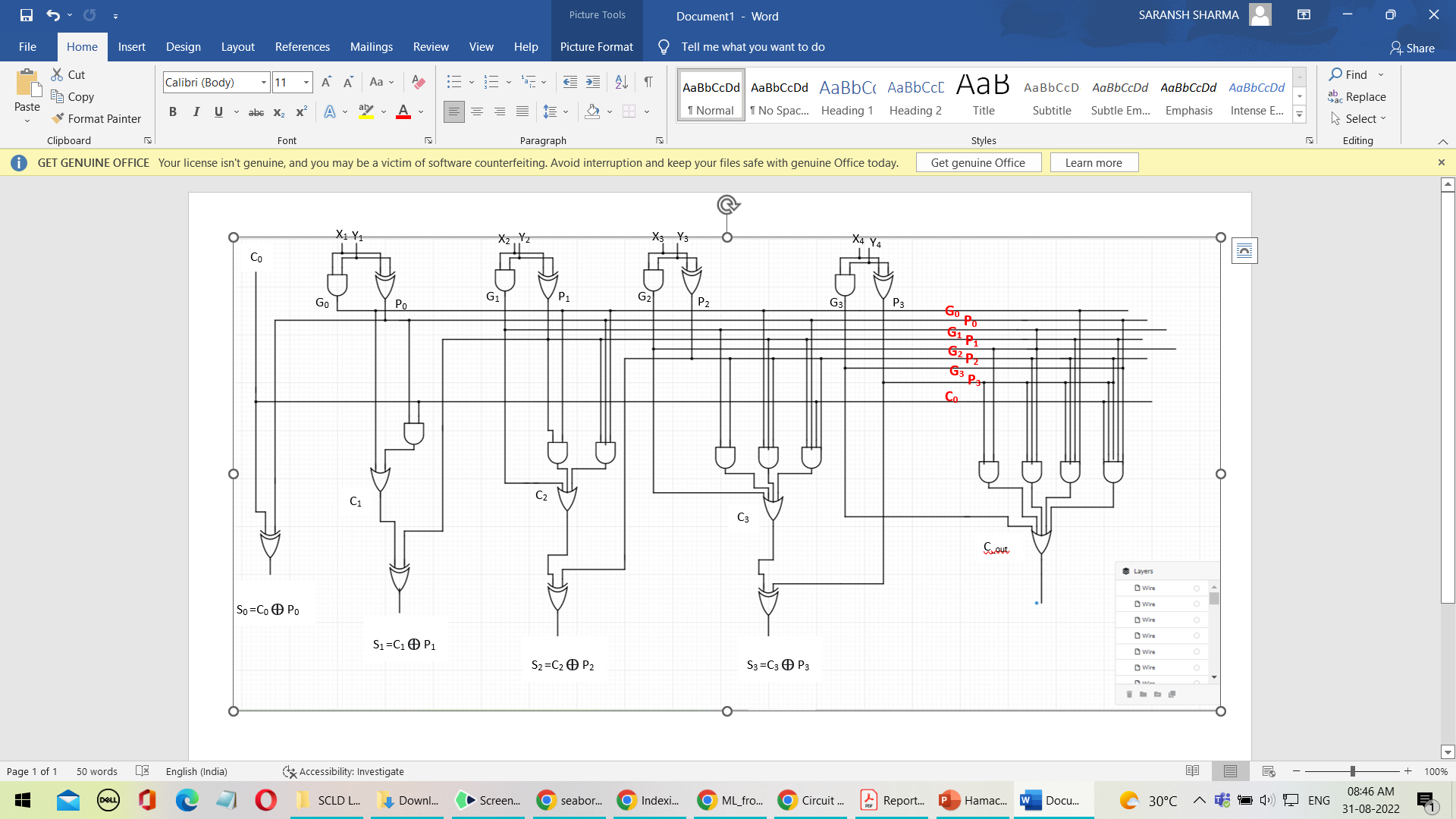
C[i+1] = G[i] + P[i]C[i]

(Notation: A & B 🡺 AB and A or B 🡺 A + B)

Upon further expanding

C[1] = G[0] + P[0]C[0]  
  
C[2] = G[1] + P[1]G[0] + P[1]P[0]C[0]  
  
C[3] = G[2] + P[2]G[1] + P[2]P[1]G[0] + P[2]P[1]P[0]C[0]  
  
C[4] = G[3] + P[3]G[2] + P[3]P[2]G[1] + P[3]P[2]P[1]G[0] + P[3]P[2]P[1]P[0]C[0]

That is all C[1], C[2], C[3], C[4] can now be represented in terms of C[0].



1. 4-Bit Carry Look Ahead Adder (augmented)

The previous circuit will be modified so that the block outputs propagate P and generate G instead of carry-out. This P and G will help us in constructing 16-Bit and higher order CLA using 4-Bit CLA.

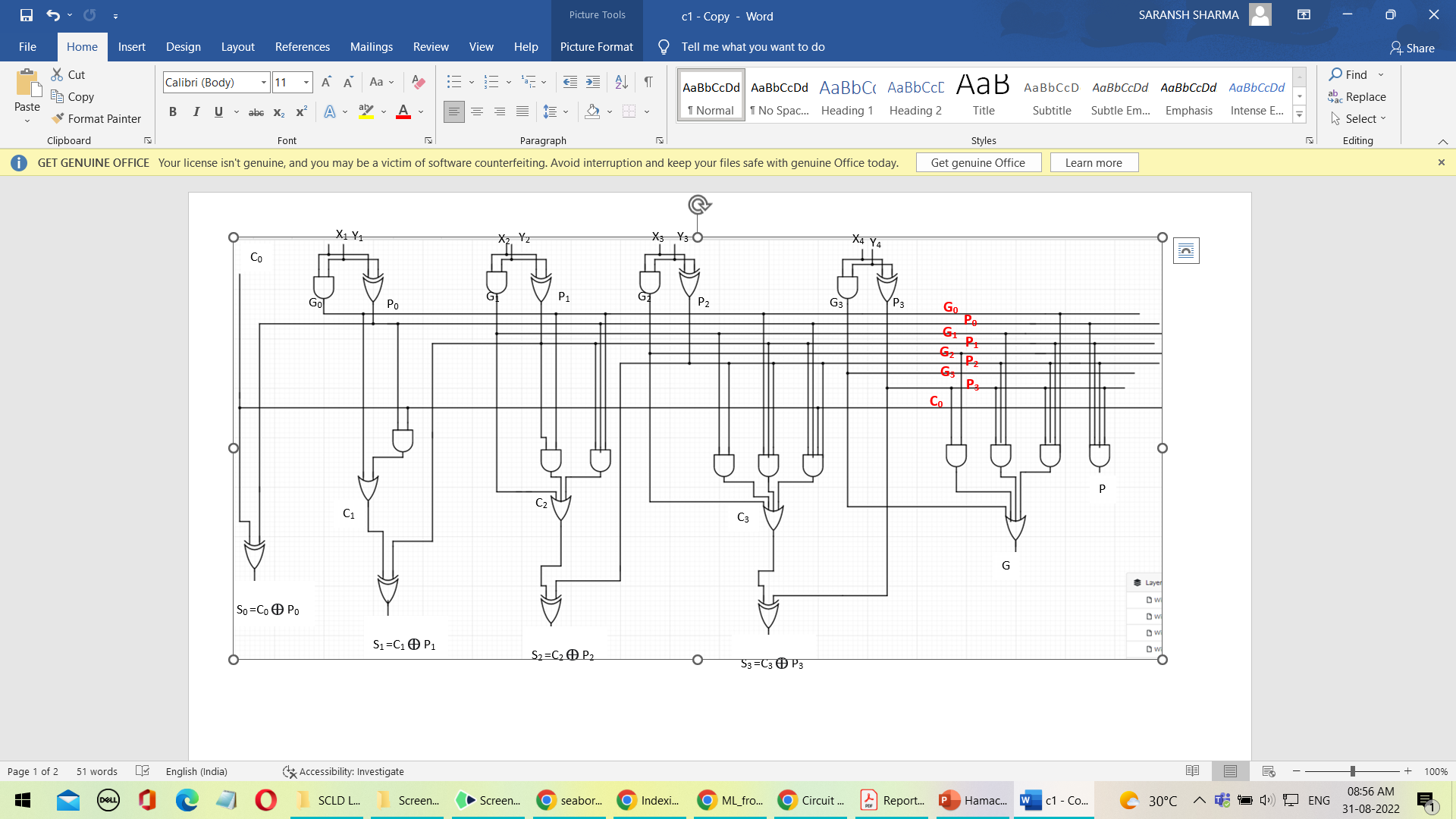
The expressions of C[i] and Sum[i] remains the same, i.e.,

Sum[i] = P[i] **⊕** C[i]

C[i+1] = G[i] + P[i]C[i]

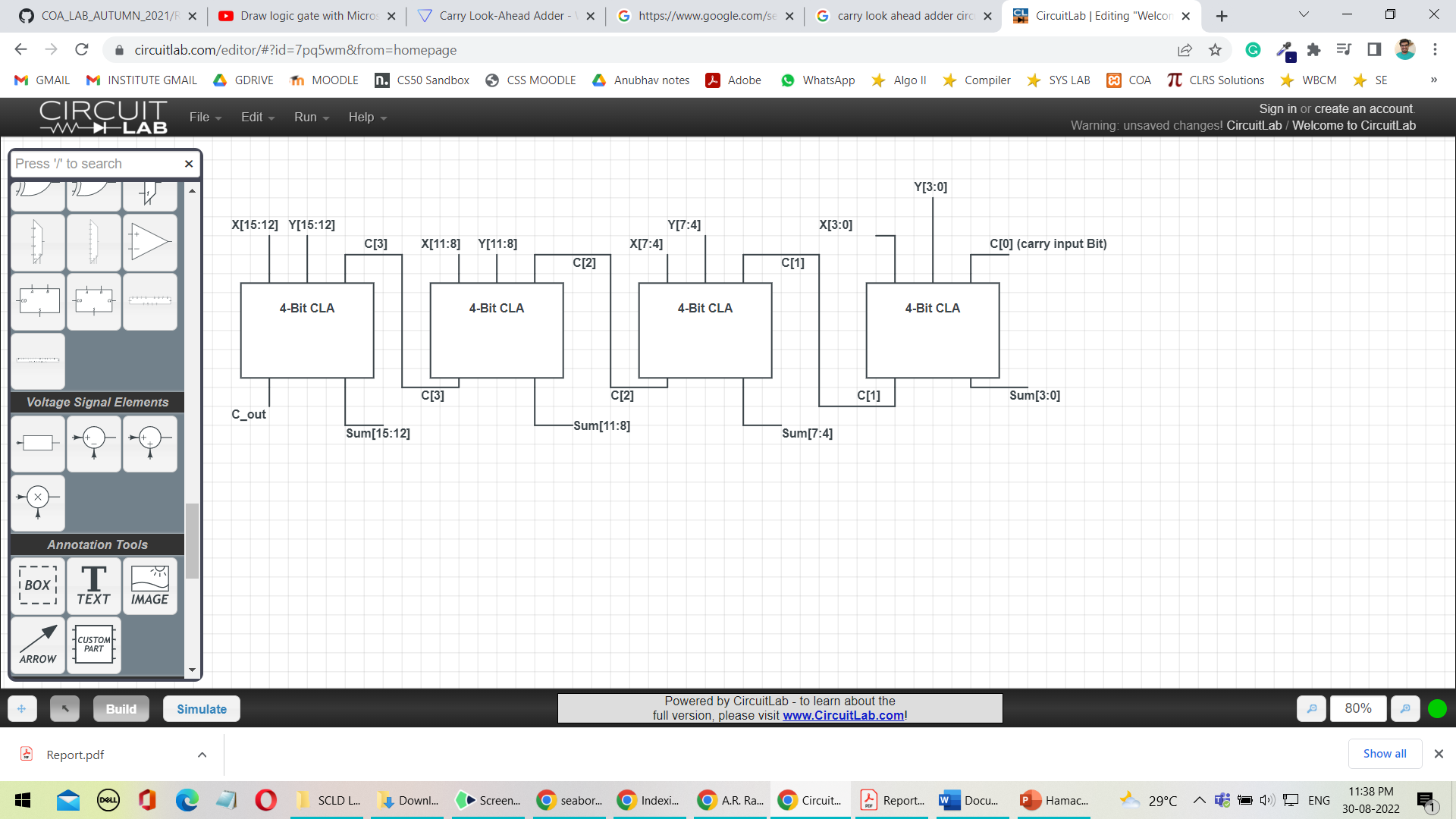
P = P[3]P[2]P[1]P[0]

G = G[3] + P[3]G[2] + P[3]P[2]G[1] + P[3]P[2]P[1]G[0] + P[3]P[2]P[1]P[0]C[0]



1. 16-Bit Carry Look-Ahead Adder

16-Bit CLA can be constructed by connecting 4 4-Bit CLA and rippling the carry of one block to the next block. C[3], C[2] and C[1] are the internal carries of the circuit.



1. 16- Bit Carry Look- Ahead Adder (Look- Ahead Carry Unit)

The previous circuit has to wait for carry from previous block to do further calculations. We can reduce this delay by using an additional look-ahead unit along with 4 CLA’s which can calculate carries using propagate and generate of the 4 CLA’s. let P[0],P[1],P[2],P[3] be the propagates of the 4 blocks of CLA and G[0],G[1],G[2],G[3] be the generates of the 4 blocks of CLA. Uisng this 16-Bit CLA, delay is further reduced and this circuit can be then used for constructing higher order CLA’s.

Equations involved:

C0 is the input carry

Sum[i] = P[i] **⊕** C[i]

C[i+1] = G[i] + P[i]C[i]

C[1] = G[0] + P[0]C[0]  
  
C[2] = G[1] + P[1]G[0] + P[1]P[0]C[0]  
  
C[3] = G[2] + P[2]G[1] + P[2]P[1]G[0] + P[2]P[1]P[0]C[0]  
  
C[4] = G[3] + P[3]G[2] + P[3]P[2]G[1] + P[3]P[2]P[1]G[0] + P[3]P[2]P[1]P[0]C[0]

Also propagate and generate of this circuit would be:

P = P[3]P[2]P[1]P[0]

G = G[3] + P[3]G[2] + P[3]P[2]G[1] + P[3]P[2]P[1]G[0] + P[3]P[2]P[1]P[0]C[0]

